IN THE DRAWINGS

Please replace Figures 2 and 6 with the attached replacement sheets.

REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-6 and 8-15 are pending. Claims 1-6 and 8-15 stand rejected.

Claims 1, 13, and 15 have been amended. No claims have been cancelled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants respectfully submit that the amendments do not add new matter.

Drawings

The Examiner stated that

> The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: $L_{met.}$ See page 9, lines 10-17.

(p. 2, Office Action 03/23/05)

Applicants respectfully submit that the Examiner inadvertently made such a statement. instead of stating that drawings do not include the reference character $L_{met.}$ mentioned in the description on page 6, lines 10-17.

Applicants submit herewith marked-up copies of drawings with a proposed correction in red, together with replacement drawings, for Figures 2 and 6 to comply with 37 CFR 1.84(p)(5). The amendments to the drawings have been made to include the reference character L_{met} mentioned in the specification in the paragraph on page 6 starting with words " The n-type region 206..." in description of Figure 2, and in the paragraph on page 16 starting with words "Yet another advantage of the lateral recess..." in description of Figure 6.

More specifically, Applicants here have amended drawings for Figures 2 and 6, to include L_{met1}, which denotes a larger physical or metallurgical channel length of the channel region directly beneath the gate dielectric, and L_{met2}, which denotes a smaller physical or metallurgical channel length of the channel region deeper into the substrate between the inflection points, as described in the specification in the above mentioned paragraphs on pages 9 and 16 with respect to Figures 2 and 6 respectively.

In the Specification

Applicants here have amended the specification to refer to a larger physical or metallurgical channel length of the channel region directly beneath the gate dielectric with the reference character L_{met1} instead of L_{met}, and to refer to a smaller physical or metallurgical channel length of the channel region deeper into the substrate between the inflection points with the reference character L_{met2} instead of L_{met}, to comply with amendments of drawings.

Rejections Under 35 U.S.C. § 112

The Examiner has rejected claims 1-6, 8-12 and 15 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. The Examiner stated that

> It is not clear how the applicant is defining the metallurgical channel length in line 14 of claim 1, for example. The claim states "inflection points which occurs between 50-200 A laterally beneath said gate electrode and at a depth of between 25-100 A beneath said gate dielectric and define a metallurgical channel length", however, the claim later states that there is a "metallurgical channel directly beneath said lower portion of said gate electrode." It appears the claim already defines the "metallurgical channel length" as being the length between the inflection points, and therefore, the region "directly beneath said lower portion of said gate electrode" can not also be called a metallurgical channel length (as per the definition already sated in the claim).

(p. 3, Office Action 032305)

Applicants here have amended claims 1 and 15 overcome the Examiner objection by indicating that said silicon or silicon alloy source/drain regions define a first channel region having a first metallurgical channel length directly beneath said lower portion of said gate electrode in said first conductivity type region, and a second channel region having a second metallurgical length between said metallurgical inflection points, wherein said first metallurgical channel length directly beneath said lower portion of said gate electrode is larger than said second metallurgical channel length between said metallurgical inflection points.

Given that claims 2-6, 8-12 depend, directly or indirectly, from amended claim 1, Applicants respectfully submit that the Examiner's objection under 35 U.S.C. § 112, second paragraph, with respect to claims 2-6, and 8-12 has been overcome.

Rejections Under 35 U.S.C. § 103(a)

Claims 1, and 8-11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,814,861 of Schunke et al. ("Schunke"). Claim 2 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Schunke in view of U.S. Patent No. 5,970,351 of Takeuchi ("Takeuchi"). Claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Schunke in view of U.S. Patent No. 6,057,582 of Choi ("Choi'582"). Claim 4 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Schunke in view Takeuchi in further view of Choi'582. Claims 5 and 6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Schunke in view of U.S. Patent No. 5,793,088 of Choi et al. ("Choi'088). Claim 12 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Schunke in view of U.S. Patent No. 5,567,966 of Hwang ("Hwang"). Claim 13 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Schunke in view of U.S. Patent No. 5,814,861 of Wieczorek et al. ("Wieczorek") in further view of Takeuchi. Claim 14

stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Schunke in view of Wieczorek, in view of Takeuchi, and in further view of Choi'582. Claim 15 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Schunke in view of Wieczorek.

Applicants have amended claim 1 to indicate that a pair of silicon or silicon alloy inwardly concaved source/drain regions of a second conductivity type is formed at opposite sides of the gate electrode in the recesses in the substrate, wherein the recesses have an inwardly concaved geometry with inflection points, such that metallurgical inflection points are created directly beneath said lower portion of said gate electrode formed directly on said gate dielectric layer. As such, a pair of silicon or silicon alloy inwardly concaved source/drain regions define a first channel region having a first metallurgical channel length directly beneath the lower portion of the gate electrode in the first conductivity type region, and a second channel region having a second metallurgical length between the metallurgical inflection points, wherein the first metallurgical channel length directly beneath the lower portion of the gate electrode is larger than the second metallurgical channel length between the metallurgical inflection points, as recited in amended claim 1.

Schunke, in contrast, discloses source/drain regions in a substrate having the depressed surface. More specifically, Schunke discloses

> Referring to FIGS. 5(a) and 5(b), a process of manufacturing a VLDD MOSFET following the step shown in FIG. 1(a), is described. FIG. 5(a) shows the gate electrode 20 formed on a p-type silicon substrate 22 with a gate dielectric film 24 interposed therebetween similar to FIG. 1(b). However, the surface of the silicon substrate 22 is depressed in the area where the source/drain regions are to be formed, relative to the level of silicon substrate in the area beneath the gate electrode 20 and gate dielectric film 24. The depressed area is formed during the same etching process for forming the gate 20 and the gate dielectric film 24, shown in FIG. 1(b).

(Schunke, col. 5, lines 7- 25) (emphasis added)

Thus, Schunke discloses source/drain regions in a depressed surface of the substrate, and not in the recesses in the substrate, wherein the recesses have an inwardly concaved geometry with inflection points, as recited in amended claim 1. Accordingly, Schunke fails to disclose, teach, or suggest the limitations of amended claim 1 of a pair of silicon or silicon alloy inwardly concaved source/drain regions of a second conductivity type formed in the recesses having an inwardly concaved geometry with inflection points in said substrate and on opposite sides of said gate electrode creating metallurgical inflection points directly beneath said lower portion of said gate electrode formed directly on said gate dielectric layer, wherein said silicon or silicon alloy source/drain regions define a first channel region having a first metallurgical channel length directly beneath said lower portion of said gate electrode in said first conductivity type region, and a second channel region having a second metallurgical length between said metallurgical inflection points, wherein said first metallurgical channel length directly beneath said lower portion of said gate electrode is larger than said second metallurgical channel length between said metallurgical inflection points.

It is respectfully submitted that Schunke does not disclose, teach, or suggest optimization of a transistor to have source/drain regions in the recesses in the substrate, which have an inwardly concaved geometry with inflection points, as recited in amended claim 1.

Furthermore, if Schunke were optimized as the Examiner suggested, to have an inflection point between 50-250Å laterally beneath the gate electrode and at a depth of between 25-100Å beneath the gate dielectric, such an optimization would still lack of source/drain regions in the recesses in the substrate, wherein the recesses have an inwardly

concaved geometry with inflection points, as recited in amended claim 1. Accordingly, such an optimization would still lack discussed above limitations of amended claim 1.

Therefore, Applicants respectfully submit that claim 1 is not obvious under 35 U.S.C. §103(a) over Schunke.

Given that claims 2-6 and 8-12 depend, directly or indirectly, from claim 1 and add additional limitations, Applicants respectfully submit that claims 2-12 are likewise not obvious under 35 U.S.C. §103(a) over Schunke.

Similarly to Schunke, neither Takeuchi, Choi'582, Choi'088, Hwang, nor Wieczorek discloses, teaches, or suggests discussed above limitations of amended claim 1.

Wieczorek merely discloses source and drain regions formed in trenches in a substrate (Wieczorek, col. 11, lines 16-43), and not in the recesses in the substrate, wherein the recesses have an inwardly concaved geometry with inflection points, as recited in amended claim 1.

Takeuchi, merely discloses elevated drain/source regions formed on a substrate, and not in the recesses in the substrate, wherein the recesses have an inwardly concaved geometry with inflection points, as recited in amended claim 1.

Choi '582, in contrast, merely discloses conventional drain/source regions formed in the surface of a substrate, and not in the recesses in the substrate, wherein the recesses have an inwardly concaved geometry with inflection points, as recited in amended claim 1.

Choi '088, in contrast, merely discloses source/drain regions in a substrate, and not in the recesses in the substrate, wherein the recesses have an inwardly concaved geometry with inflection points, as recited in amended claim 1.

Hwang, in contrast, discloses elevated source/drain regions in a substrate, and not in the recesses in the substrate, wherein the recesses have an inwardly concaved geometry with inflection points, as recited in amended claim 1.

Hence, none of the references cited by the Examiner discloses, teaches, or suggests the limitations of claim 1 of a pair of silicon or silicon alloy inwardly concaved source/drain regions of a second conductivity type formed in the recesses having an inwardly concaved geometry with inflection points in said substrate and on opposite sides of said gate electrode creating metallurgical inflection points directly beneath said lower portion of said gate electrode formed directly on said gate dielectric layer, wherein said silicon or silicon alloy source/drain regions define a first channel region having a first metallurgical channel length directly beneath said lower portion of said gate electrode in said first conductivity type region, and a second channel region having a second metallurgical length between said metallurgical inflection points, wherein said first metallurgical channel length directly beneath said lower portion of said gate electrode is larger than said second metallurgical channel length between said metallurgical inflection points.

Consequently, even if Schunke, Takeuchi, Choi'582, Choi'088, Hwang, and Wieczorek were combined, such a combination would lack such limitations of amended claim 1.

Therefore, Applicants respectfully submit that amended claim 1 is not obvious under 35 U.S.C. § 103 (a) over the references cited by the Examiner.

Given that claims 2-6 and 8-12 depend from amended claim 1, either directly or indirectly, and add additional limitations, Applicants respectfully submit that claims 2-6 and 8-12 are not obvious under 35 U.S.C. §103 (a) over all the references cited by the Examiner.

Because amended independent claims 13 and 15 contain at least the same limitations as amended claim 1, Applicants respectfully submit that claims 13 and 15 are likewise not obvious under 35 U.S.C. §103(a) over all the references cited by the Examiner.

Given that claim 14 depends directly from claim 13 and add additional limitations, applicants respectfully submit that claim 14 is likewise not obvious under 35 U.S.C. §103(a) over all the references cited by the Examiner.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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Date: June 22, 2005

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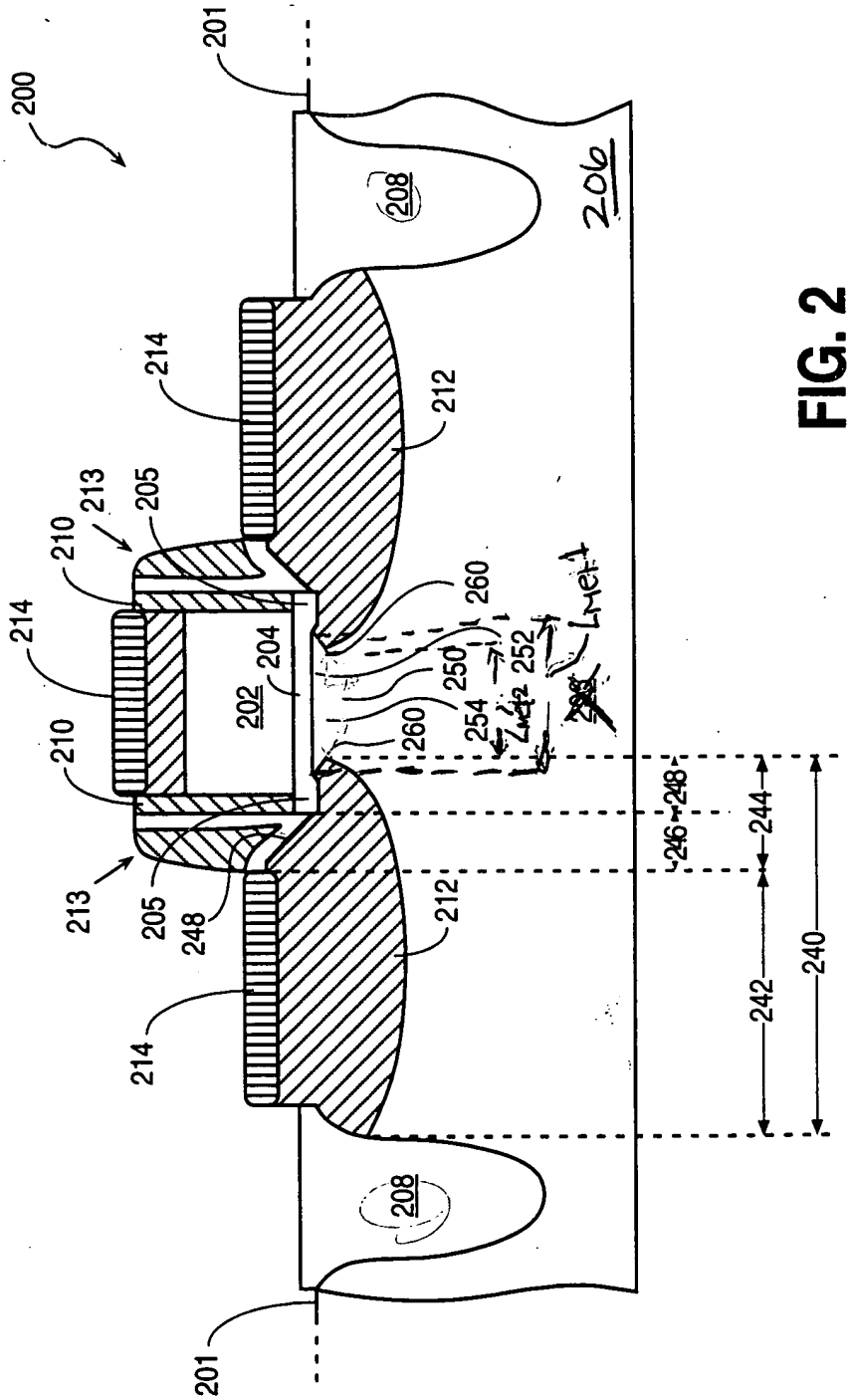

FIG. 2

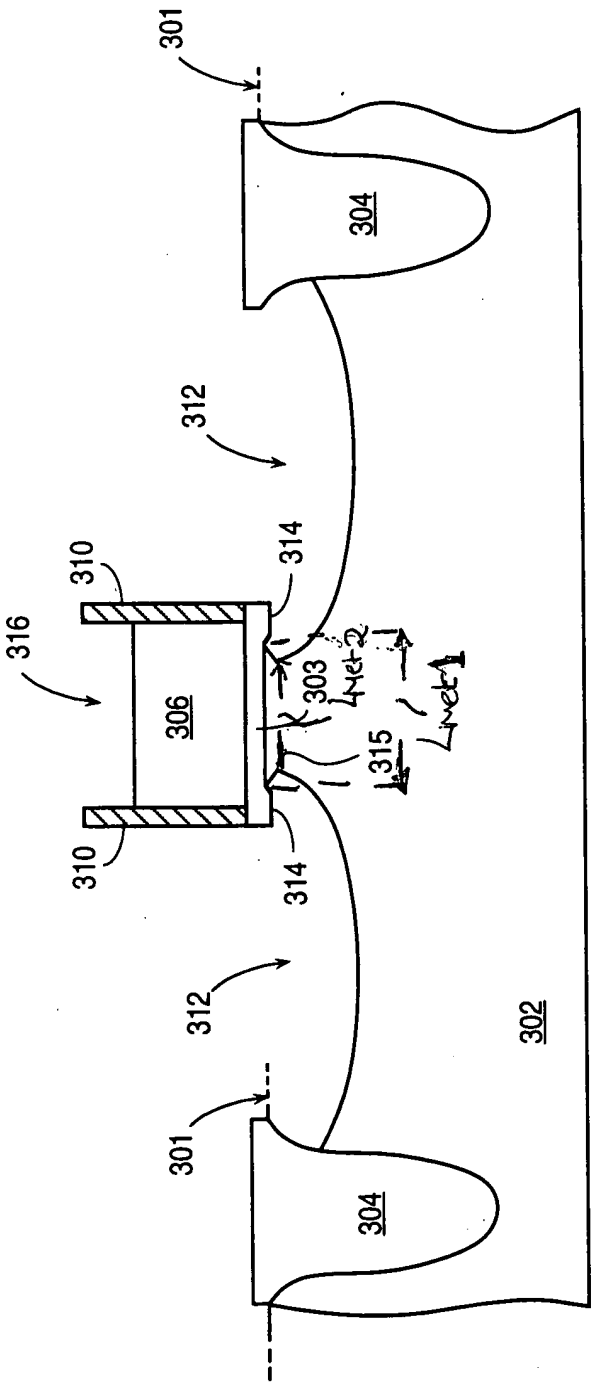

FIG. 6